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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/085,757	02/27/2002	Bo Soon Chang	CYPR-PM01008	8405

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EXAMINER	
JARRETT, RYAN A	
ART UNIT	**PAPER NUMBER**
2125	

DATE MAILED: 02/05/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/085,757	CHANG, BO SOON	
	Examiner	Art Unit	
	Ryan A. Jarrett	2125	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 February 2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-49* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-49* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. Figure 1 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

This objection is based on the Applicant's disclosure on page 3 of the specification, which states, "An embodiment of a ***conventional*** batch-oriented back-end IC manufacturing process is illustrated in Figure 1."

Information Disclosure Statement

2. Applicant is advised to submit an IDS containing the references listed on page 21 of the provisional application filed 2/27/01.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

4. Claims 1-4, 6, 8, and 9 are rejected under 35 U.S.C. 102(a) as being clearly anticipated by applicant's Admitted Prior Art (Fig. 1, pg. 3 line 4 – pg. 7 line 20). There is no recitation in any of the above claims of an automatic transfer device (e.g. conveyor) residing between the different assembly line portions.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 10-16, 18, 20, 21, 23, 24, 26, 27, and 29-36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Admitted Prior Art as applied to claim 1 above, and further in view of Jin et al. U.S. Patent No. 6,392,286 (Admission-Jin). Admission discloses an IC back-end manufacturing assembly comprising: a front-of-line portion comprising a plurality of sub-stations for operating on a plurality of die-strips in an in-line basis commencing with an in-line die attach sub-station and ending with a in-line plasma sub-station; and an end-of-line portion receiving processed die-strips from said front-of-line portion in an in-line fashion and comprising a plurality of sub-stations for operating on said processed die-strips in an in-line basis commencing with an in line mold sub-station and ending with a sort sub-station; further comprising: an in-line test portion receiving die-strip components output from said in-line sort sub-station and for testing said die-strip components; and a finish portion coupled to said in-line test portion and comprising a plurality of sub-stations operating on tested die-strip components output from said in-line test portion and commencing with a marking sub-station and ending with a tape and reel sub-station; wherein one of said plurality of sub-stations of said front-of-line portion further comprises another in-line plasma sub-station; wherein one of said plurality of sub-stations of said front-of-line portion is an in-line snap cure

substation; wherein one of said plurality of sub-stations of said front-of-line portion is an in-line bond substation; wherein said plurality of sub stations of said end-of-line portion further comprise: an in-line post mold cure sub-station coupled to said in-line mold sub-station; an in-line solder ball attachment sub-station; and an in-line sawing sub-station coupled to said sort sub-station; wherein said plurality of substations of said finish portion further comprise a final visual inspection sub-station coupled between said marking sub-station and said tape and reel sub-station (Fig. 1, pg. 3 line 4 – pg. 7 line 20);

an apparatus for automatically performing back-end fabrication of an IC device comprising: (a) a die attach module adapted to attach a plurality of IC die to a substrate under computer control; (b) a bonding module adapted to bond wires to both the substrate and the attached die under computer control; (c) a molding module adapted to encapsulate bonded die and substrate with a mold material under computer control; (d) a singulation module adapted to separate encapsulated, bonded die and substrate under computer control into separated die; (e) a testing module adapted to test the separated die under computer control; and (f) a plurality of transporters adapted to transport: (i) the substrate and the attached die from the die attach module to the bonding module; (ii) the bonded die and substrate from the bonding, module to the molding module; (iii) the encapsulated, bonded die and substrate from the molding module to the singulation module; and (iv) the separated die from the singulation module to the testing module; further comprising a marking module adapted to mark the tested die under computer control; further comprising a packaging module adapted to

package the tested die under computer control to produce packaged die; wherein the packaging module comprises a tape and reel module; further comprising a snap curing module adapted to snap cure an adhesive adapted to attach the plurality of die to the substrate; further comprising an in-line plasma cleaning module adapted to plasma clean the substrate and attached die; further comprising an in-line plasma cleaning module adapted to plasma clean the bonded substrate and die; wherein the singulation module comprises a sawing module; further comprising a sawing module adapted to saw wafers under computer control to provide said separated die (Fig. 1, pg. 3 line 4 – pg. 7 line 20).

In the Admission, the transporters consist of human operators that transfer the workpieces between the various assembly line modules. There is no disclosure in the Admission of any type of automatic transfer device, such as a conveyor, that transfers the workpieces between the assembly line modules. However, Jin discloses a semiconductor chip packaging system comprising a conveyor that automatically transports semiconductor die between various assembly line modules in an in-line fashion, the modules comprising sawing equipment, die attach equipment, cleaning tools, wire bonding equipment, molding equipment, and singulation equipment. Each of the assembly equipments includes a loading part and an unloading part. Jin also discloses that the substrate holding the die comprises an n-by-m matrix array ball grid array (BGA) substrate and wherein n and m each independently being an integer of at least 2 (e.g. Figs. 1-4, col. 1 lines 7-20, col. 3 lines 55 – col. 4 line 6, col. 4 lines 26-31, col. 5 lines 19-54, col. 9 lines 10-35, col. 9 line 61 – col. 10 line 67, col. 11 line 25 – col.

12 line 14). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the Admission with Jin since Jin teaches that an automatic conveyor can speed up processing and eliminate the need for an extra operator (e.g. col. 4 lines 26-31).

7. Claims 5 and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Admission as applied to claims 4 and 6 above, and further in view of Farnsworth et al. U.S. Patent No. 6,549,821 (Farnsworth). The Admission discloses multiple manual visual inspection stations located on the assembly line. The Admission does not disclose the use of camera systems for performing automated die-strip inspections at the die attach, bond, mold, solder ball attachment, or sorting substations. However, Farnsworth discloses a method for packaging electronic components. The process sequence comprises die attach, bond, mold, solder ball attach, test, marking, and packaging modules (e.g. Fig. 9). Farnsworth also discloses a camera/automated machine vision system adapted to inspect the encapsulated, marked, bonded die and substrate (e.g. col. 4 line 59 – col. 5 line 11, col. 6 line 35-55, col. 9 line 60 – col. 11 line 6). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Admission with Farnsworth since Farnsworth teaches that an automatic machine vision system can be used in a back-end semiconductor assembly line to eliminate the precise mechanical alignment of workpieces that was necessary in the prior art. Accordingly, accurate workpiece alignment and material disposition can be reliably obtained (e.g. col. 4 line 59 – col. 5 line 4).

8. Claims 17, 19, 22, 25, 28, and 37-48 are rejected under 35 U.S.C. 103(a) as being unpatentable over Admission-Jin as applied to claims 12, 18, 21, 24, and 27 above, and further in view of Farnsworth et al. Admission-Jin discloses most all of the features of these claims as detailed above. Admission-Jin does not disclose cameras or automated machine vision systems adapted to inspect the die at the various assembly line substations. However, Farnsworth discloses a method for packaging electronic components. The process sequence comprises die attach, bond, mold, solder ball attach, test, marking, and packaging modules (e.g. Fig. 9). Farnsworth also discloses a camera/automated machine vision system adapted to inspect the encapsulated, marked, bonded die and substrate (e.g. col. 4 line 59 – col. 5 line 11, col. 6 line 35-55, col. 9 line 60 – col. 11 line 6). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Admission-Jin with Farnsworth since Farnsworth teaches that an automatic machine vision system can be used in a back-end semiconductor assembly line to eliminate the precise mechanical alignment of workpieces that was necessary in the prior art. Accordingly, accurate workpiece alignment and material disposition can be reliably obtained (e.g. col. 4 line 59 – col. 5 line 4).

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Tuttle et al. U.S. Patent No. 6,045,652

Wensel U.S. Patent No. 6,230,719

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ryan A. Jarrett whose telephone number is (703) 308-4739. The examiner can normally be reached on 10:00-6:30 M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Leo Picard can be reached on (703) 308-0538. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Ryan A. Jarrett
Examiner
Art Unit 2125

2/2/04

LEO PICARD
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100